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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,657	03/29/2004	Chih-Ta Wu	67,200-1255	2448

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EXAMINER	
TRINH, MICHAEL MANH	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/811,657	WU ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's amendment filed on March 30, 2006. Claims 1-20 are pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 1-4,9-11,13-15 are rejected under 35 U.S.C. 102(a)/(e) as being anticipated by Agarwal et al (6,596,583).

Re claims 1,9, Otsuki teaches a method for forming an MIM capacitor, in which the capacitor electrodes is deposited by using a thermal CVD or ALD deposition process, which is a plasma-free deposition process, thereby preventing plasma induced damage to the capacitor dielectric, which method comprising: providing a substrate (63 in Fig 9B; 32 in Fig 8A) ; providing a capacitor opening in said substrate; providing a bottom electrode in the capacitor opening (65 in Fig 9B, 26 in Fig 8A; col 7, lines 44-67; Figs 1-7; col 4, line 12 through col 6); thermally annealing the bottom electrode (col 7, lines 44-66); providing a capacitor dielectric layer (69 in Fig 9B, 28 in Fig 8A) in the capacitor opening on said bottom electrode; and depositing a top electrode (70/71 in Fig 9B, col 8, lines 51-67; col 9, lines 1-32; 30 in Fig 8A) on said capacitor dielectric layer by using a deposition process such as a thermal CVD or an atomic layer deposition (ALD) (col 7, lines 30-43), which thermal CVD or ALD deposition process is a plasma-free deposition process, thereby preventing plasma induced damage to the capacitor dielectric, inherently, wherein, re further claims 9, the capacitor dielectric layer is a high-k dielectric layer (col 8, lines 1-21). Re claims 2,4,10,14, wherein the top electrode

deposited using a thermal CVD deposition process using tungsten fluoride and ammonia or ALD is substantially organic-free content (col 7, lines 44-60; col 8, lines 22-32). Re claims 3,11,15, wherein annealing the bottom electrode comprises exposing the bottom electrode to nitrogen gas while subjecting the bottom electrode to thermal process (col 7, lines 44-67). Re claim 13, wherein the electrode is deposited by using thermal CVD or ALD deposition process (col 7, lines 30-43) which is plasma-free deposition process.

Claim Rejections - 35 USC § 103

3. Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al (6,596,583) taken with Iizuka (2002/0190294).

Agarwal et al teach a method for forming an MIM capacitor as applied to claims 1-4, 9-11,13-15 above, and fully incorporated herein. Agarwal also teaches, re further claim 17, that, the capacitor dielectric layer is a high-k dielectric layer (col 8, lines 1-21), and wherein the top electrode comprising TiN deposited on the capacitor high-k dielectric layer (col 8, lines 22-32, 1-21); Re further claim 18, wherein the top electrode deposited using a thermal CVD deposition process using tungsten fluoride and ammonia or ALD is substantially organic-free content (col 7, lines 44-60; col 8, lines 22-32); and Re further claim 19, wherein annealing the bottom electrode comprises exposing the bottom electrode to nitrogen gas while subjecting the bottom electrode to thermal process (col 7, lines 44-67).

Re claim 17, Agarwal already teaches forming a capacitor structure having a bottom electrode in co-planar with the substrate capacitor opening, but lacks mentioning about subjecting the bottom electrode to chemical mechanical planarization.

However, Iizuka also teaches (at Figs 7-8;9I-9J; paragraph 87; 112,100-112) forming and subjecting a bottom lower electrode 34 to a chemical mechanical planarization (CMP).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a capacitor structure of Agarwal by subjecting the bottom electrode to a chemical mechanical planarization (CMP), as taught by Iizuka. This is because of the desirability to form a planar and thin capacitor structure as the electrodes are recessed in an opening of an insulating layer, in which chemical mechanical planarization (CMP) is an effective and reliable process for forming a capacitor device having planar structure.

4. Claims 5-8,12,16,20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al (6,596,583) as applied to claims 1-4,9-11,13-15 above, with Iizuka (2002/0190294) as applied to claims 17-19 above, taken with Otsuki et al (6,919,273) and Basceri et al (2004/0046197).

Agarwal et al teach a method for forming an MIM capacitor as applied to claims 1-4,9-11,13-15 above. Agarwal and Iizuka (2002/0190294) as applied to claims 17-19 above. Re claims 6,8, wherein the top electrode deposited using a thermal CVD deposition process using tungsten fluoride and ammonia or ALD is substantially organic-free content (col 7, lines 44-60; col 8, lines 22-32). Re claim 7, wherein annealing the bottom electrode comprises exposing the bottom electrode to nitrogen gas while subjecting the bottom electrode to thermal process (col 7, lines 44-67).

Re claims 5,12,16,20, Agarwal already teaches using thermal CVD or ALD deposition process for forming the electrode, but lacks mentioning a temperature of no greater than about 400°C.

However, Otsuki et al teaches (at col 9, lines 1-12; lines 1-56) using a thermal CVD deposition process for forming the electrode at a low temperature of 200-500°C, preferably of 200°C, which temperature of 200°C is no greater than about 400°C. Basceri also teaches (at paragraphs 0074, 0061, and 0071) depositing the electrode by using ALD or CVD at low deposition temperature, preferably at a deposition process temperature of about 400°C which temperature is no greater than about 400°C.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the top electrode of Agarwal by deposition using thermal CVD or ALD deposition process for forming the electrode at a low temperature of 200-500°C, preferably of 200°C, which temperature of 200°C is no greater than about 400°C. Basceri also teaches (at paragraphs 0074, 0061, and 0071) depositing the electrode by using ALD or CVD at low deposition temperature, preferably at a deposition process temperature of about 400°C.

The subject matter as a whole would have been obvious to one or ordinary skill in the art at the time the invention was made to form the top electrode of Agarwal by selecting the portion of the prior art's range of temperature, as taught by Agarwal and Basceri, which is within the

range of applicant's claims, because it has been held to be obvious to select a value in a known range by optimization for the best results. *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948); *In Re Swanson* 56 USPQ 372 (CCPA 1942); *In Re Sola* 25 USPQ 433 (CCPA 1935); and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934). Also, this is because of the desirability to prevent the formation of additional oxygen vacancies in the capacitor dielectric material such as aluminum oxide, which typically occur as a result of high processing temperature (Basceri, paragraphs 0071).

5. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Otsuki et al (6,919,273) taken with Olewine et al (2003/0067023) and Iizuka (2002/0190294).

Re claims 1,9,17, Otsuki teaches a method for forming an MIM capacitor, comprising: providing a substrate; providing a capacitor opening in said substrate (Figs 2-8); providing a bottom electrode (67 in Fig 7, col 10, lines 16-52); 62,63 in Figs 5-6,8,4; col 9, line 50 through col 10) in said capacitor opening; providing a capacitor dielectric layer 64 on said bottom electrode; and depositing a top electrode (66 in Figs 7,6; 65/68 in Figs 5,8) on said dielectric layer 64. Re claims 2,4,6,8,10,14, wherein the top electrode 66 deposited from thermal CVD by using $TiCl_4$ is substantially organic-free content (col 7, lines 56 through col 8; col 6, line 65 through col 7, lines 55). Re claims 5,12,16, wherein the electrode is deposited at a temperature including about 400°C (col 14, lines 30-35; col 8,lines 35-41). Re further claims 9,13, as similarly applied to claim 1, wherein the electrodes are deposited by thermal CVD deposition so that it is plasma-free deposition process (col 6, line 65 through col 8). Re further claims 17,19, Olewine already teaches (at paragraphs 55; 50-58; Figs 1-5) annealing a capacitor bottom electrode of TiN with nitrogen prior to deposition of the insulation layer of the capacitor (re claim 17,19). Re claim 18, wherein the top electrode 66 deposited from thermal CVD by using $TiCl_4$ is substantially organic-free content (col 7, lines 56 through col 8; col 6, line 65 through col 7, lines 55). Re claim 20, wherein the electrode is deposited at a temperature including about 400°C (col 14, lines 30-35; col 8,lines 35-41).

Re claims 1,9,17, Otsuki already teaches forming the bottom electrode and forming a capacitor dielectric on the bottom electrode, but lacks annealing the bottom electrode with

nitrogen (re further claims 3,7,11,15,19), and providing the capacitor dielectric layer in the opening.

However, Olewine also teaches (at paragraphs 55; 50-58; Figs 1-5) annealing a capacitor bottom electrode of TiN with nitrogen prior to deposition of the insulation layer of the capacitor. Iizuka teaches (at col 7, lines 44-60; col 8, lines 22-32) forming a MIM capacitor, wherein the method is employed to form several alternative capacitor structures as shown in Figures 7-8, Figure 9L, Figure 11, and Figure 12, wherein, in one embodiment of Figs 7-8,9L, the capacitor dielectric layer (15 in Figs 7-8; 35 in Fig 9L) is provided in the capacitor opening on the bottom electrode (13 in Figs 7-8; 34 in Fig 9L) instead of forming the capacitor electrode layer on the bottom electrode above the substrate (Figs 11-12). Olewine also teaches (at paragraphs 55; 50-58; Figs 1-5) annealing a capacitor bottom electrode of TiN with nitrogen prior to deposition of the insulation layer of the capacitor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the capacitor of Otsuki by annealing the bottom electrode of TiN with nitrogen as taught by Olewine. This is because of the desirability to treat the TiN electrode layer to reduce or eliminate oxidation of the surface prior to and during deposition of the dielectric layer of the capacitor. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form another capacitor structure for Otsuki by providing the capacitor dielectric layer in the capacitor opening on the bottom electrode as taught by Iizuka as shown in Figs 8 and 9L. This is because of the desirability to form a trench capacitor structure in the capacitor opening formed in the substrate, thereby forming a thin integrated device as the capacitor is recessed down and buried in the substrate.

Re further claim 17, the references including Otsuki and Iizuka teach forming a trench capacitor structure having the bottom electrode as applied to claims 1-16 above. Claim 17 further recites subjecting the bottom electrode to a chemical mechanical planarization.

However, Iizuka also teaches (at Figs 7-8;9I-9J; paragraph 87; 112,100-112) forming and subjecting a bottom lower electrode 34 to a chemical mechanical planarization (CMP).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a capacitor structure of the references including Otsuki by subjecting the bottom electrode to a chemical mechanical planarization (CMP), as taught by Iizuka. This is

because of the desirability to form a planar and thin capacitor structure as the electrodes are recessed in an opening of an insulating layer.

Response to Amendment

6. Applicant's remarks filed March 30, 2006 with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

Moreover, in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the references prima facie obviously teach the claimed invention. Iizuka clearly teaches subjecting the bottom capacitor electrode to chemical mechanical polishing so as to form a planar capacitor structure having the bottom electrode recessed in the capacitor opening.

Further, claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In Re Self, 213 USPQ 1,5 (CCPA 1982); In Re Priest, 199 USPQ 11,15 (CCPA 1978).

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Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs-16

Michael Trinh
Primary Examiner